APPENDIX

1. A semiconductor memory apparatus comprising:

a memory unit **(10)**[2] having a plurality of unit blocks **(11)**, wherein each unit block includes:

a memory core including a plurality of memory cells laid out to form a cell matrix **[0043]**, **[0045]**; and

redundant lines **(14)**, **(15)** including redundant memory cells **(11)** each used for repairing an abnormal memory cell generated in any of said memory cores,

wherein said plurality of unit blocks **(11)** form a block matrix or a plurality of block matrixes, and each of said plurality of unit blocks forms a one-dimensional group oriented in a first direction (row or column direction) or a second direction (column or row direction) **[0043]**, ***See*** **Fig. 2**; and

said redundant lines **(14)**, **(15)** are shared by a group of said plurality of unit blocks, wherein the group of said plurality unit blocks have a common orientation of said one-dimensional group **[0044]**;

self-test means **(20)** for evaluating said memory cells to determine whether said memory cells are abnormal, wherein said self-test means is mounted in the same chip as said memory unit **[0045]**; and

self-repair means **(30)** for receiving address pairs associated with an abnormal memory cell from said self-test means,

selecting a minimum number of address pairs of the plurality of address pairs received from said self-test means, wherein each address pair includes a first-direction address (row or column address) and a second-direction address (column or row address) associated with the abnormal memory cell **[0046]**,

storing said selected minimum number of address pairs in first storage means for each of said plurality of unit blocks required to determine a redundant line to be used to repair the abnormal memory cell **[0046]**; and

finding a redundant line to repair the abnormal memory cell based on address pairs stored in said first storage means **[0048]**.

---

[2] Numeral enclosed in parentheticals ( ) indicates element number found in drawings.

2. The semiconductor memory apparatus according to claim 1, wherein:

said self-repair means has a first storage unit **(421)** and a first shift-register unit **(422) [0046]**;

said first storage unit is capable of storing a maximum number of second-direction addresses selected from the address pairs stored in said first storage means for each unit block in said group of unit blocks of said one-dimensional group, wherein each unit forms said one-dimensional group commonly oriented in said second direction and said redundant lines connected in said second direction are shared by each unit block of said one-dimensional group **[0046]**;

said first shift-register unit has a plurality of shift registers, wherein the number of the plurality of shift registers equals the number of said redundant lines connected in said second direction **[0077]**;

each of said shift registers has as many shift stage bits as said maximum number **[0077]**; and

said first shift-register unit sequentially points to one of said second-direction addresses stored in said first storage unit by shifting the plurality of shift registers **[0082]**; and

said first shift-register unit generates an address set of said second-direction address for each unit block by operating only one of said plurality of shift registers at a time **[0091]**.

3. The semiconductor memory apparatus according to claim 2, wherein:

the address set generated as an address set of a second-direction address is reported for each unit block and, if the address pair including said second-direction address exists in said first storage means, said address pair is an address pair that can be repaired by using a redundant line connected in said second direction **[0084]**; and

if an address pair remaining in said first storage means is unrepaired, said remaining address pair is examined to determine whether said remaining address pair is repairable by using a redundant line connected in said first direction **[0086]**.

4. The semiconductor memory apparatus according to claim 3, wherein:

as means to determine whether or not it is possible to use a redundant line connected in said first direction for repairing the remaining address pair that cannot be repaired by using a redundant line connected in said second direction, said self-repair means includes a plurality of second storage units that store a first-direction address, wherein a number of said second storage units equals a number of said redundant lines connected to each unit block in said first direction **[0088]**; and

said self-repair means executes the steps of:

supplying a first-direction address of the remaining address pair that cannot be repaired by using a redundant line connected in said second direction to said second storage units **[0088]**;

discarding said first-direction address of said remaining address pair when said first-direction address has already been stored in said second storage units **[0088]**;

determining that said remaining address pair can be repaired by using a redundant line connected in said first direction when said first-direction address is stored in said second storage units **[0088]**; and

determining that said remaining address pair cannot be repaired by using a redundant line connected in said first direction when said first-direction address is not stored in said second storage units **[0088]**.

5. The semiconductor memory apparatus according to claim 3, wherein:

as means to determine whether it is possible to use a redundant line connected in said first direction for repairing the remaining address pair that cannot be repaired by using a redundant line connected in said second direction, said self-repair means is provided with a plurality of first-direction shift registers wherein the number of first-direction shift registers corresponds to the number of redundant lines connected to each of said unit blocks in said first direction **[0091]**; and

said self-repair means executes the steps of:

shifting at least one of said first-direction shift registers and taking a first-direction address pointed to by said first-direction shift registers as a first-direction repair address **[0091]**;

determining whether the remaining address pair that cannot be repaired by using a redundant line connected in said second direction, can be repaired by using a redundant line connected in said first direction as a redundant line corresponding to said first-direction repair address **[0091]**; and

further shifting at least one of said first-direction shift registers and determining whether said remaining address pair can be repaired if said remaining address pair cannot be repaired by using said redundant line connected in said first direction **[0091]**.

6. The semiconductor memory apparatus according to claim 2, wherein said shift registers of said first shift-register unit each have an additional shift stage bit that indicates a state in which redundant lines connected in said second direction are ignored **[0084]**.

7. The semiconductor memory apparatus according to claim 2,

wherein the plurality of said shift registers employed in said first shift-register unit include at least a first shift register, a second shift register, and a third register **[0091]**,

wherein when said first shift register is fixed following a shift in said second shift register and said third shift register, said first shift register is shifted by 1 bit and an operation to shift said second shift register is started from a shift-stage position coinciding with a new shift-stage position of said first shift register or a shift-stage position immediately following said new shift-stage position of said first shift register, and an operation to shift said third shift register is started from a shift-stage position coinciding with said start shift-stage position of said

second shift register or a shift-stage position immediately following said start shift-stage position of said second shift register **[0091]**.

8. The semiconductor memory apparatus according to claim 1,

wherein each of said unit block forms a one-dimensional group in said second direction, and said first storage means includes a plurality of shift register flags associated with the address pairs stored in said first storage means, wherein the number of shift-register flags corresponds to the number of said redundant lines connected to each unit block commonly oriented in said second direction of said one-dimensional group **[0092]**;

wherein said plurality of shift-register flags are linked to each other to form a chain spread over each unit block as said redundant lines connected in said second direction **[0092]**;

wherein said plurality of shift registers form a second shift-register unit; and

wherein an address set of said second-direction address is generated by successively shifting each shift register of said plurality of shift registers **[0092]**.

9. The semiconductor memory apparatus according to claim 8, wherein said plurality of shift registers of said second shift-register unit have an additional shift stage bit that indicates a state in which redundant lines connected in said second direction are ignored **[0095]**.

10. CANCELED

11. The semiconductor memory apparatus according to claim 8, wherein:

wherein said self-repair means has a duplication flag associated with each address pair of the plurality of address pairs stored in said first storage means **[0053]**;

wherein said duplication flags indicate that a corresponding address pair includes a second-direction address stored in at least two storage locations of said first storage means **[0053]**; and

wherein when at least one of said plurality of shift registers of said second shift-register unit is shifted to a next shift stage position coinciding with one of said duplication flags, which have been put in a set state, said next shift stage position is ignored and said particular shift register is shifted again **[0053]**.

12. The semiconductor memory apparatus according to claim 11, wherein:

said self-repair means reports a second-direction address pointed to by said shift registers of said second shift-register unit for each unit block **[0053]**; and

when said reported second-direction address exists in said first storage means for at least two of said unit blocks, said duplication flag of one of said at least two unit blocks is set **[0053]**.

13. The semiconductor memory apparatus according to claim 8, wherein:

said self-repair means reports to each unit block a second-direction address pointed to by said second shift-register unit while shifting said second shift-register unit **[0095]**;

when a duplicate second-direction address of said reported second-direction address exists in said first storage means, said self-repair means determines that an address pair including said same second-direction address is a repairable address pair **[0096]**;

said self-repair means first determines whether a remaining address pair is repairable **[0096]**; and

said embedded self-repair means again shifts said second shift-register unit and again determine whether said remaining address pair are repairable when a remaining address pair cannot be repaired based on the first determination **[0097]**.

14. The semiconductor memory apparatus according to claim 8, wherein said self-repair means has a special flag for each address pair of the plurality of address pairs of each unit block stored in said first storage means to indicate that a second-direction address of at least one address pair associated with said special flag matches an address set of the second-direction address reported by said embedded self-repair means for each unit block and the at least one address pair is regarded as a second-direction repair address **[0062]**.

15. – 18. CANCELED